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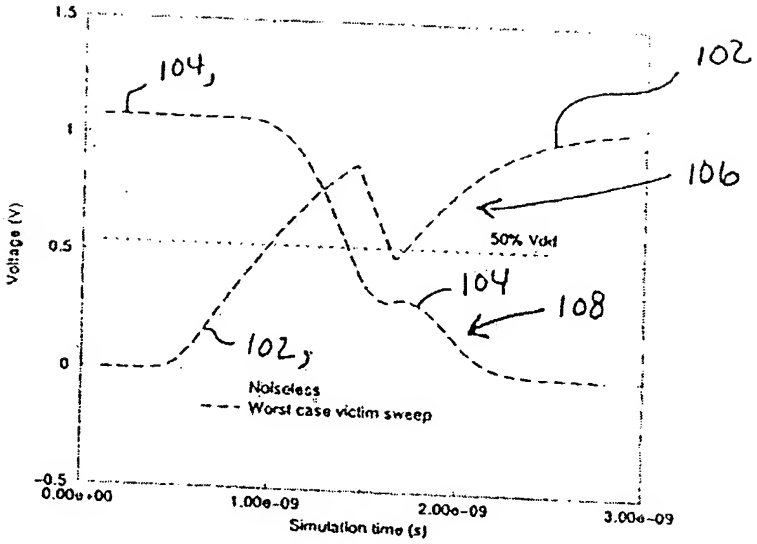

1.5
1
0.5
0
-0.5
Voltage (V)
0.00e+00
1.00e-09
2.00e-09
3.00e-09
Simulation time (s)
50% Vdd
Noiseless
Worst case victim sweep
104
102
106
104
108
102

FIGURE 1

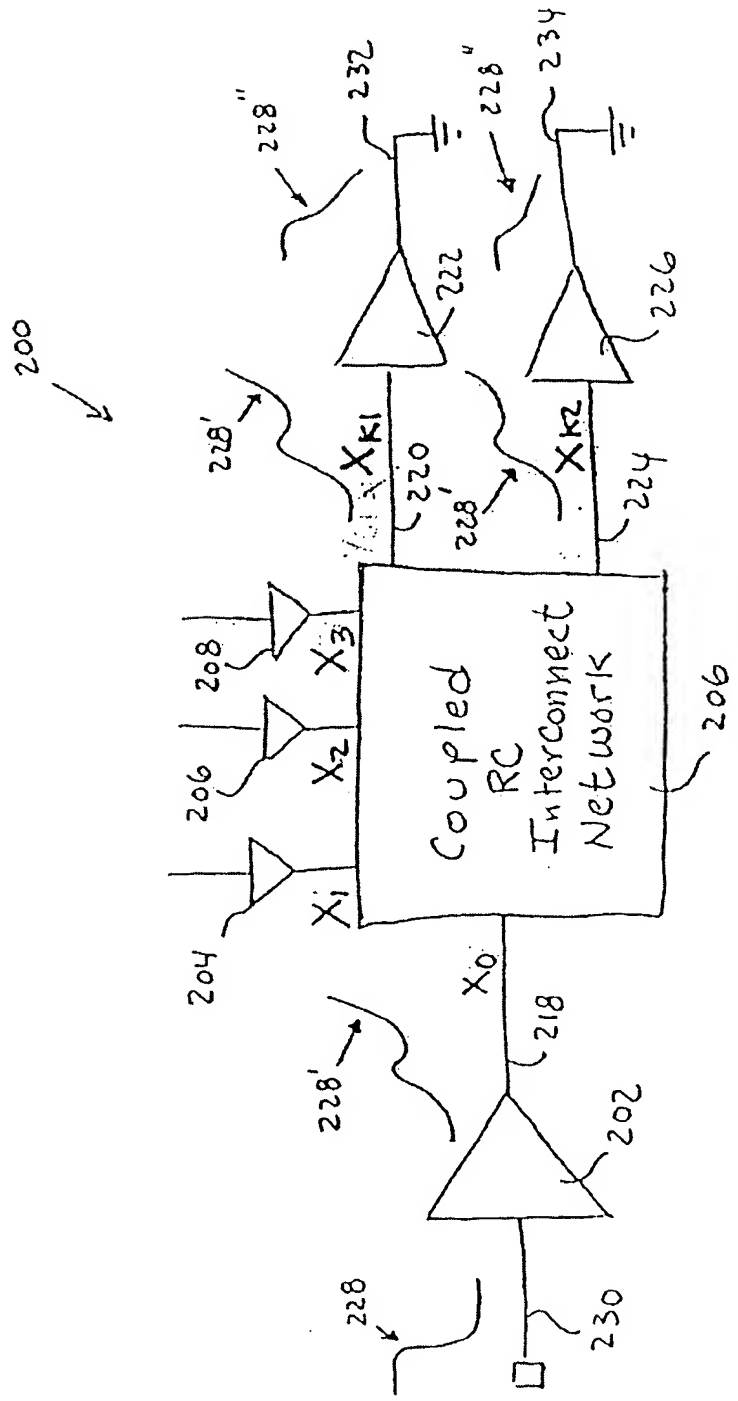

200
228''
232
228''
234
222
226
228'
X_{K1}
220
228'
X_{K2}
224
208
X_3
206
X_2
Coupled RC Interconnect Network
206
204
X_1
X_0
218
228'
202
228
230

FIGURE 2

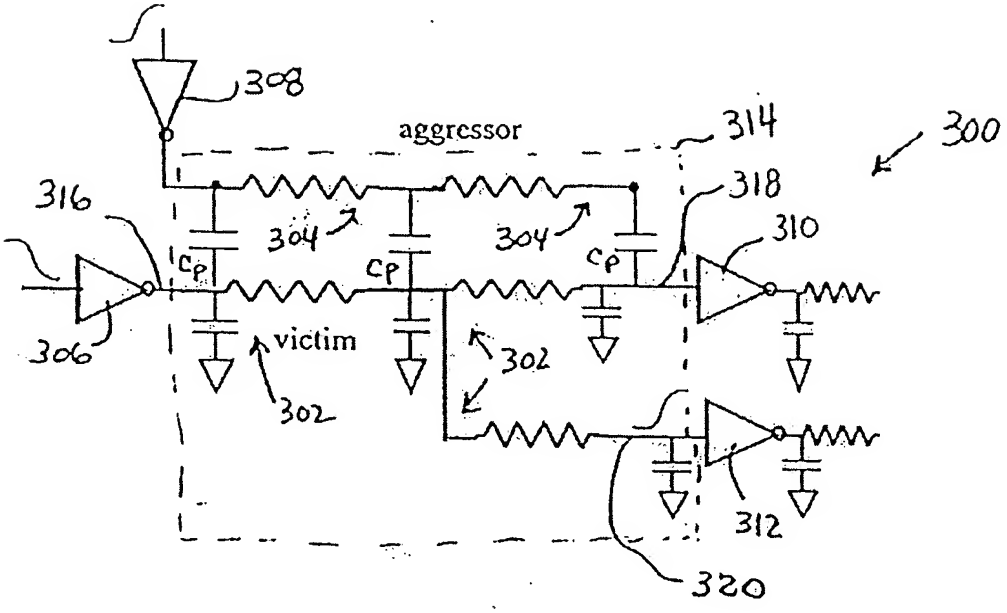

308
aggressor
314
300
316
318
304
304
310
Cp
Cp
Cp
306
victim
302
302
312
320

FIGURE 3

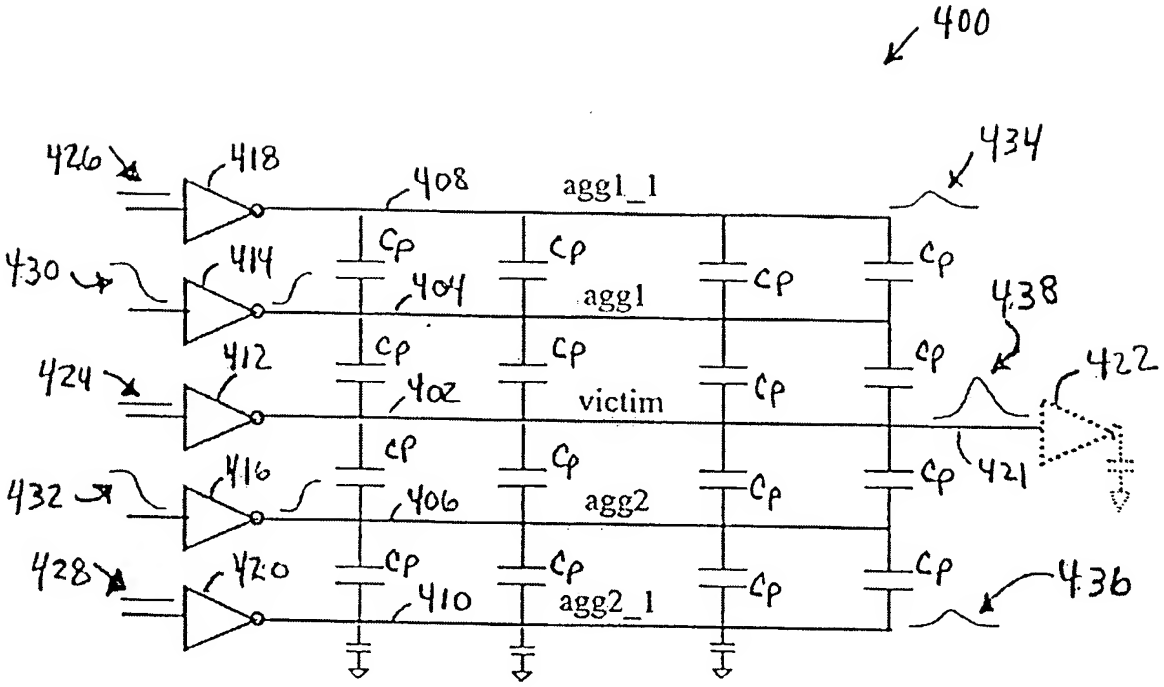

400
426
418
408
agg1_1
434
Cp
430
414
404
agg1
438
424
412
402
victim
422
421
432
416
406
agg2
428
420
410
agg2_1
436

FIGURE 4

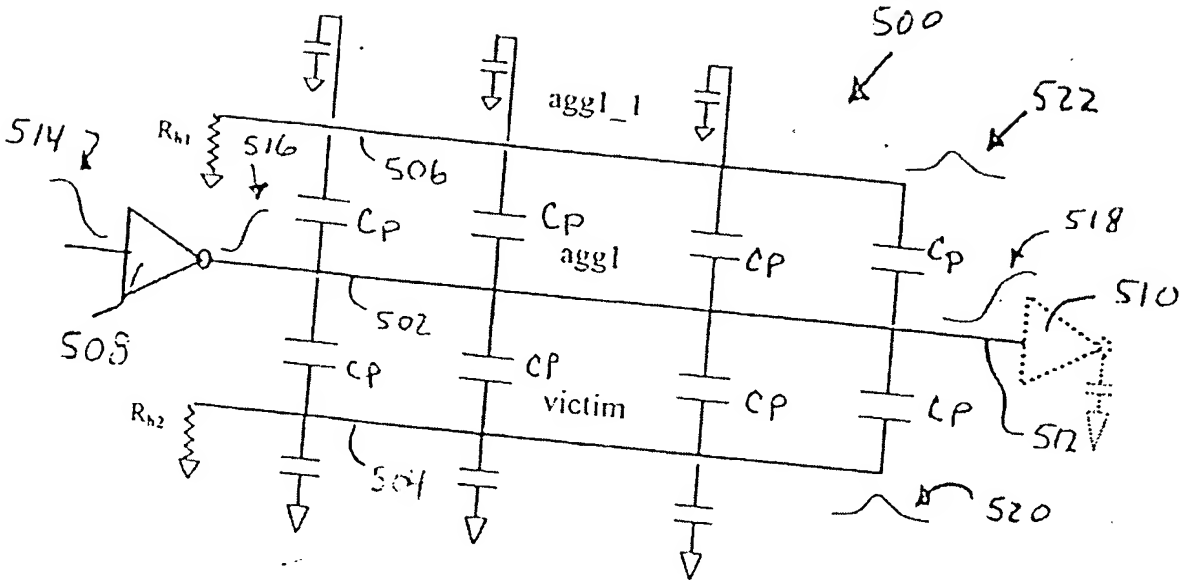

500
522
514
R_{h1}
516
506
aggl_1
Cp
Cp
aggl
Cp
Cp
518
510
505
502
Cp
Cp
victim
Cp
Cp
R_{h2}
504
512
520

FIGURE 5

Figure 6A:

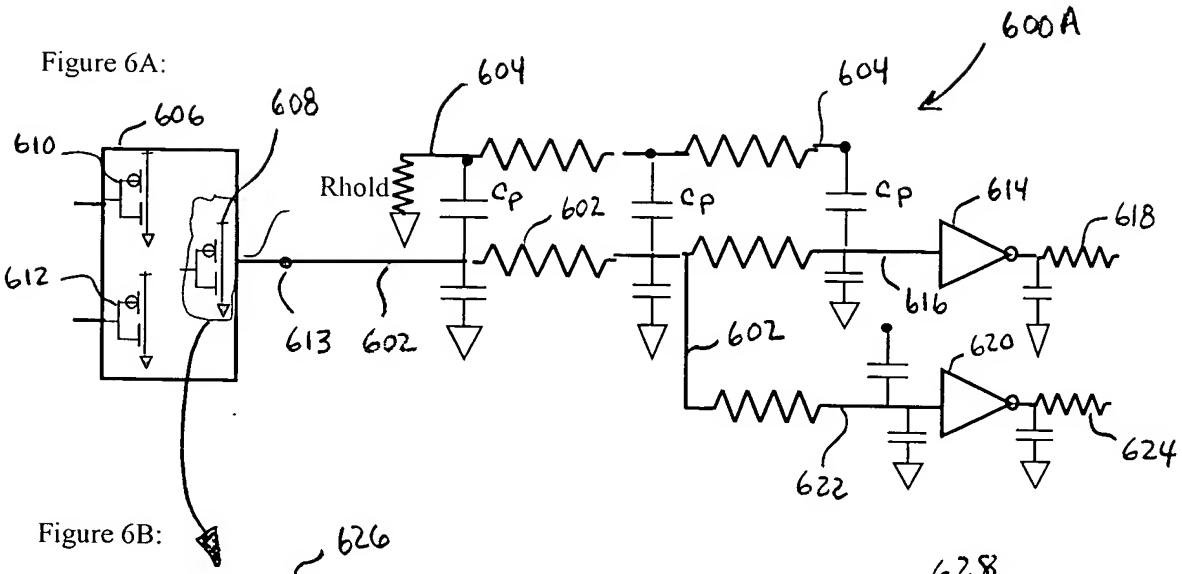
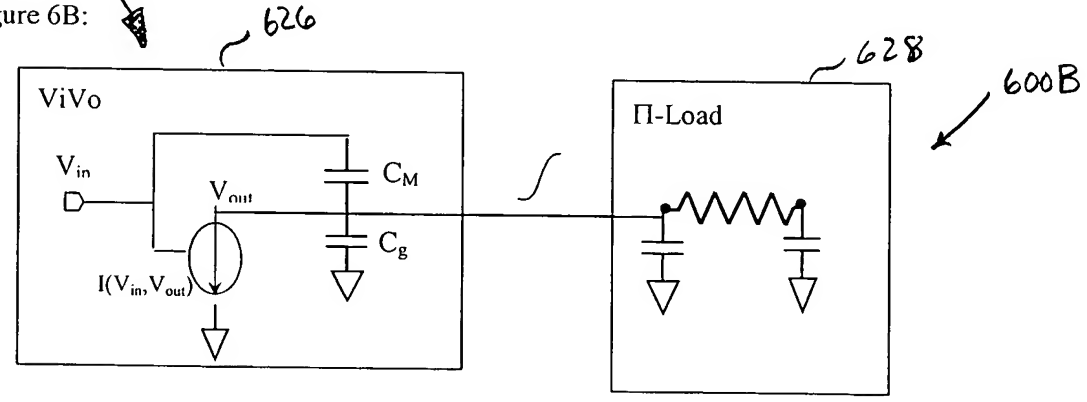


Figure 6B:



V_{in}/V_{out}	V_{o0}	V_{o1}	V_{o2}	...	V_{oN}
V_{i0}	I_{00}	I_{01}	I_{02}	...	I_{0N}
V_{i1}	I_{10}	I_{11}	1_{12}	---	I_{1N}
V_{i2}	I_{20}	I_{21}	I_{22}	---	I_{2N}
. . .	. . .	. . .	. . .	. . .	. . .
V_{iM}	I_{M0}	I_{M1}	I_{M2}	...	I_{MN}

FIGURE 7

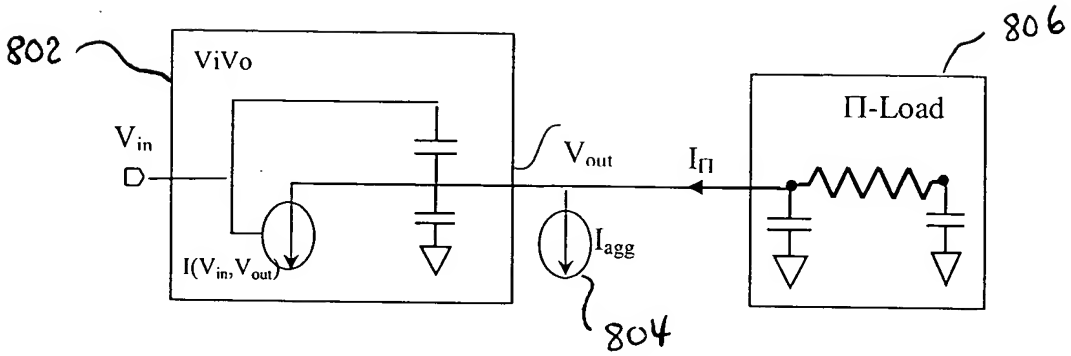


Figure 8

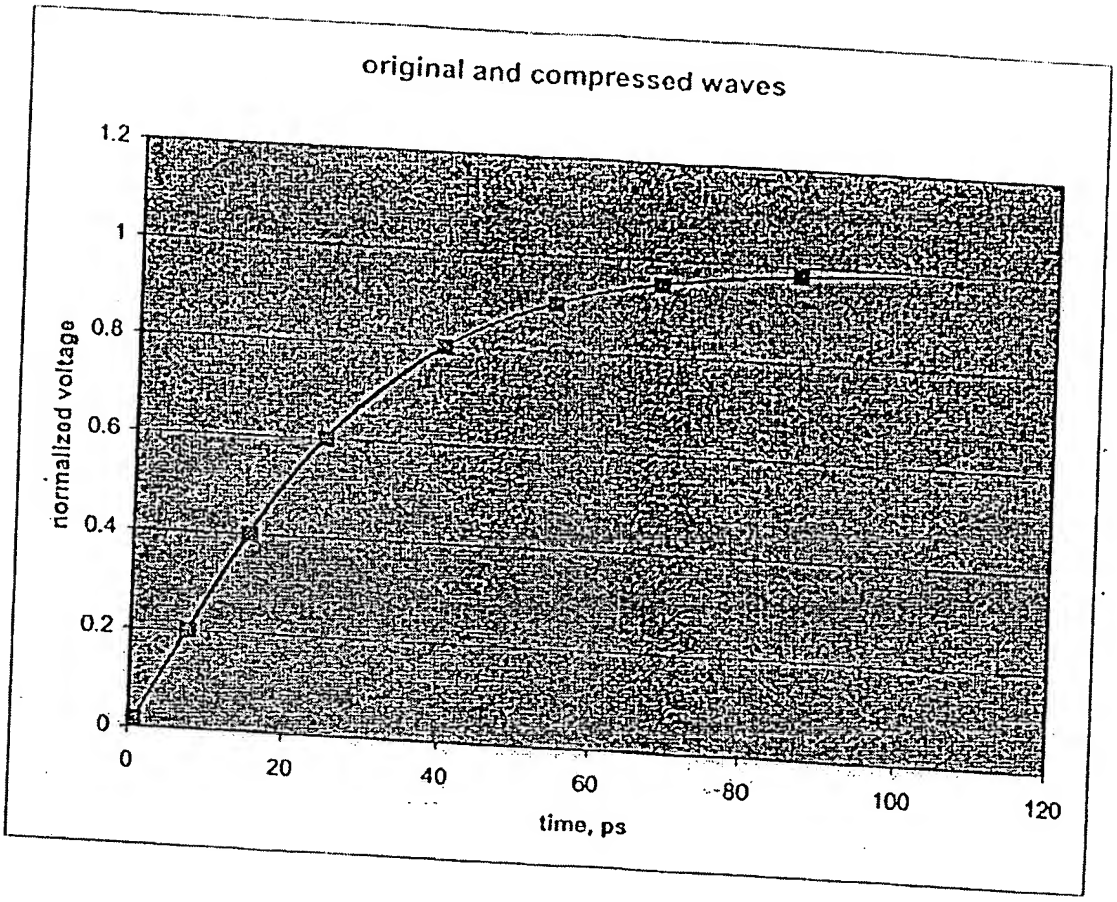

original and compressed waves
normalized voltage
1.2
1
0.8
0.6
0.4
0.2
0
0
20
40
60
80
100
120
time, ps

FIGURE 9

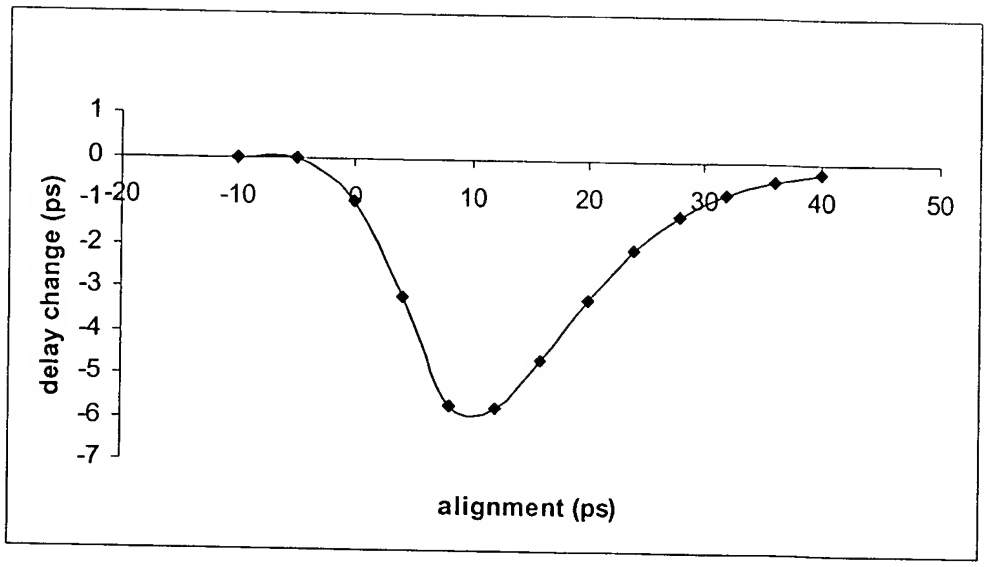


Figure 10

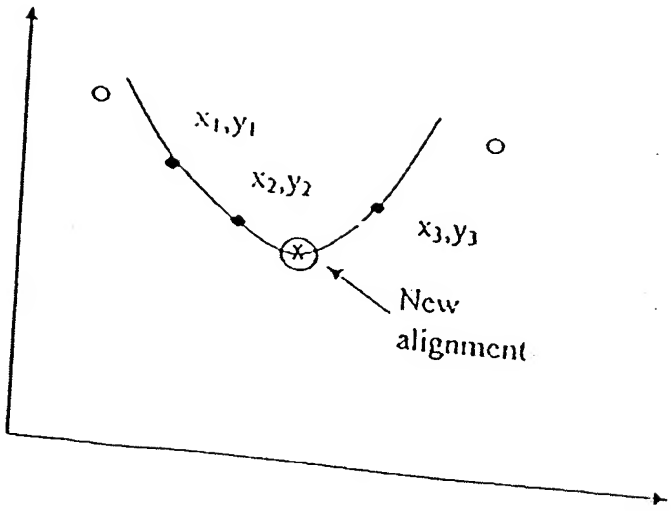


FIGURE 11

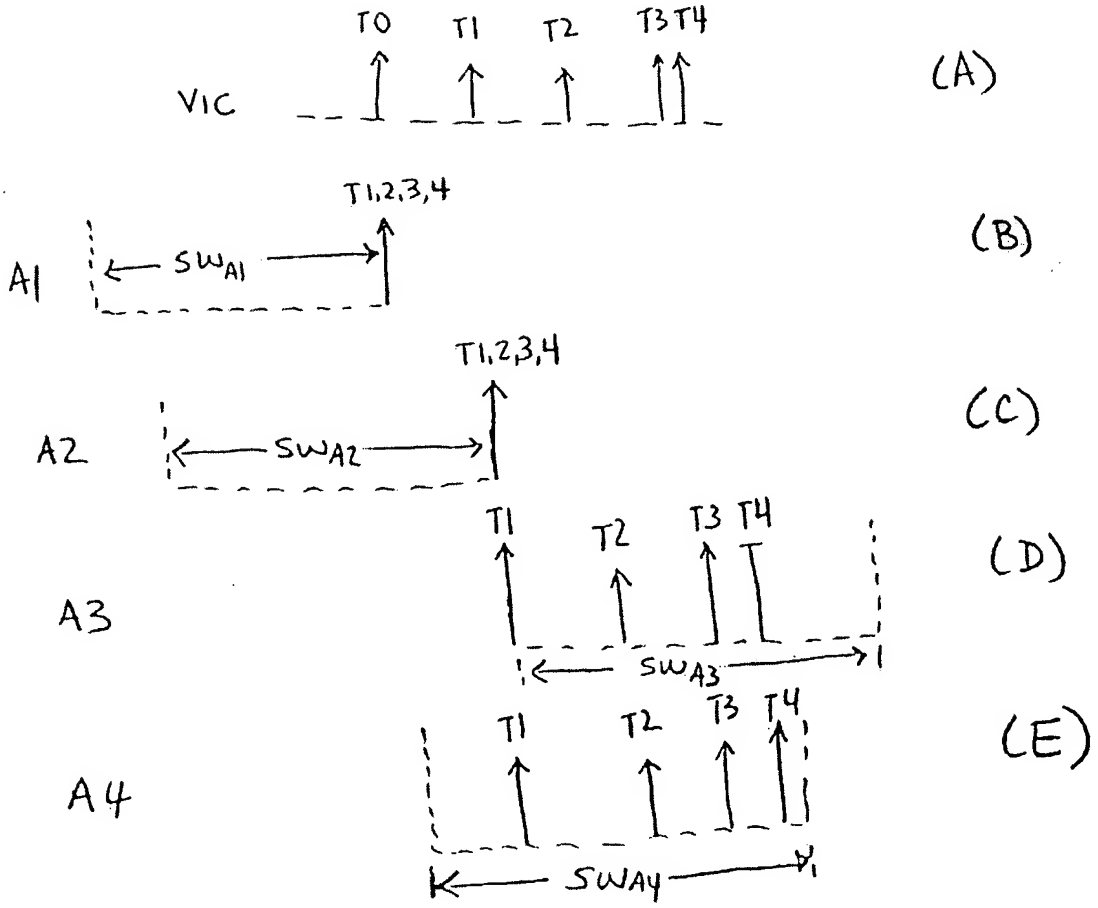

T0
T1
T2
T3 T4
VIC
(A)
T1,2,3,4
A1
SWA1
(B)
T1,2,3,4
A2
SWA2
(C)
T1
T2
T3
T4
A3
SWA3
(D)
T1
T2
T3
T4
A4
SWA4
(E)

FIGURE 12

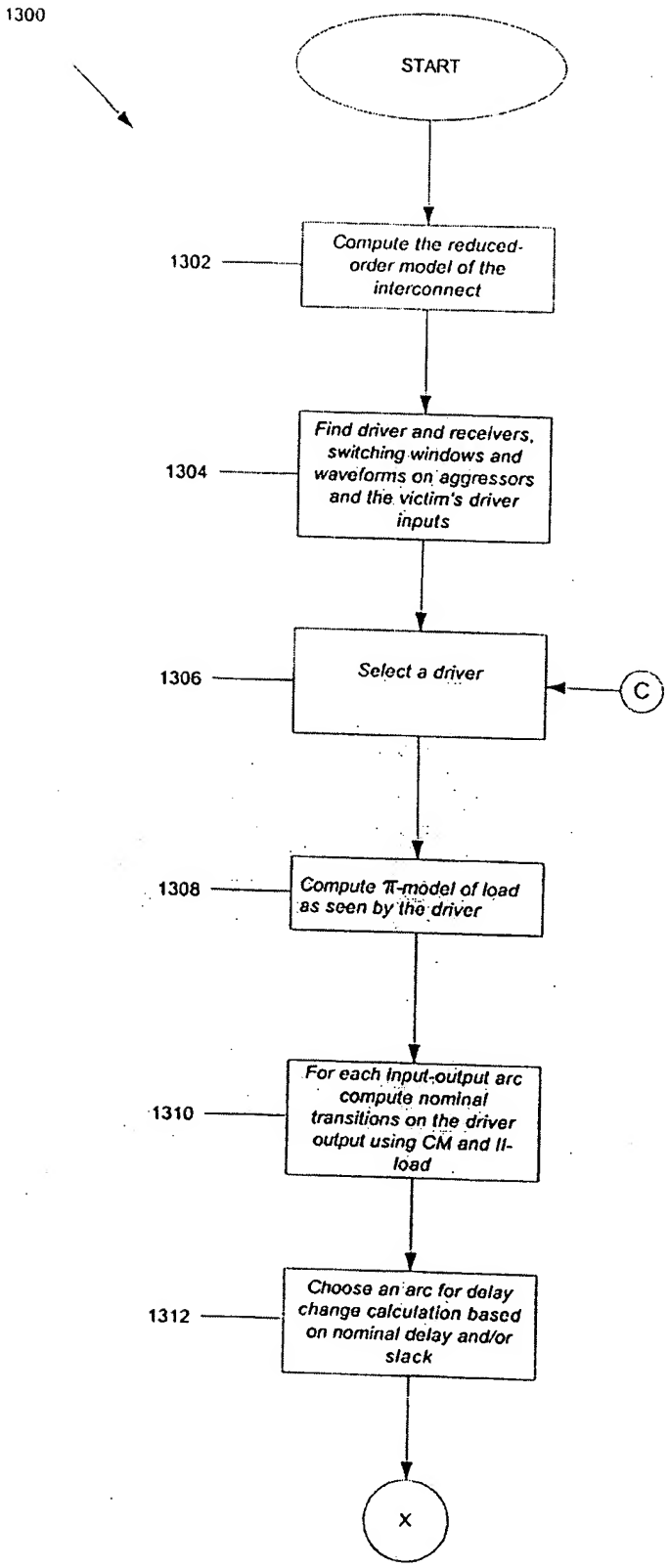

1300
START
1302
Compute the reduced-order model of the interconnect
1304
Find driver and receivers, switching windows and waveforms on aggressors and the victim's driver inputs
1306
Select a driver
C
1308
Compute π-model of load as seen by the driver
1310
For each input-output arc compute nominal transitions on the driver output using CM and II-load
1312
Choose an arc for delay change calculation based on nominal delay and/or slack
X

Figure 13A

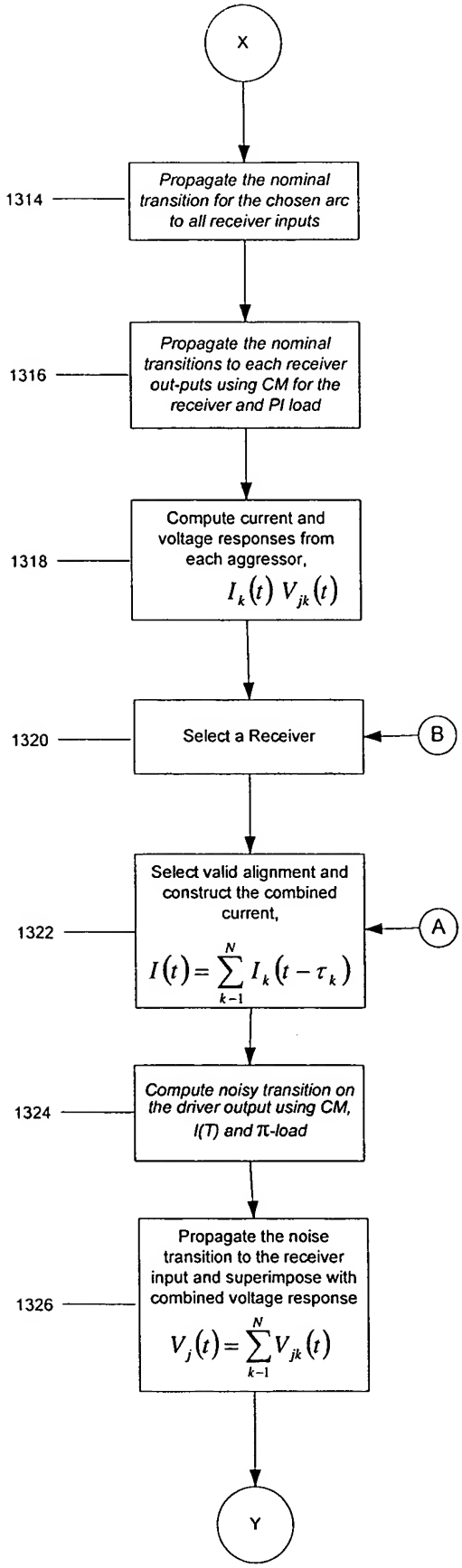

X
1314
Propagate the nominal transition for the chosen arc to all receiver inputs
1316
Propagate the nominal transitions to each receiver out-puts using CM for the receiver and PI load
1318
Compute current and voltage responses from each aggressor, $I_k(t)\ V_{jk}(t)$
1320
Select a Receiver
B
1322
Select valid alignment and construct the combined current, $I(t)=\sum_{k-1}^{N} I_k(t-\tau_k)$
A
1324
Compute noisy transition on the driver output using CM, I(T) and π-load
1326
Propagate the noise transition to the receiver input and superimpose with combined voltage response $V_j(t)=\sum_{k-1}^{N} V_{jk}(t)$
Y

Figure 13B

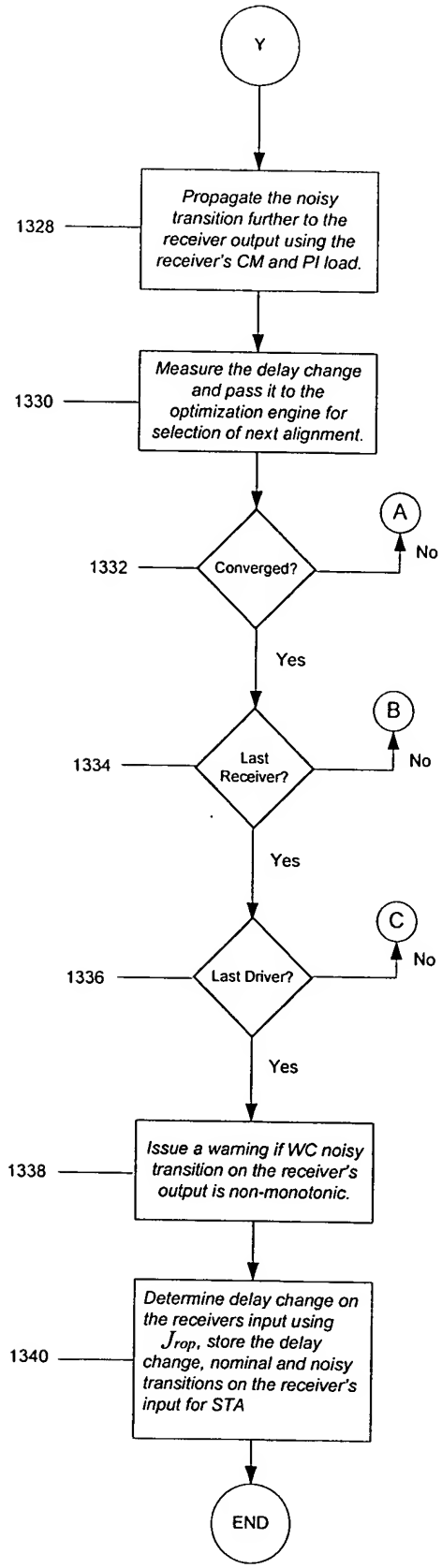

Y
1328
Propagate the noisy transition further to the receiver output using the receiver's CM and PI load.
1330
Measure the delay change and pass it to the optimization engine for selection of next alignment.
A
1332
Converged?
No
Yes
B
1334
Last Receiver?
No
Yes
C
1336
Last Driver?
No
Yes
1338
Issue a warning if WC noisy transition on the receiver's output is non-monotonic.
1340
Determine delay change on the receivers input using J_{rop}, store the delay change, nominal and noisy transitions on the receiver's input for STA
END

Figure 13C

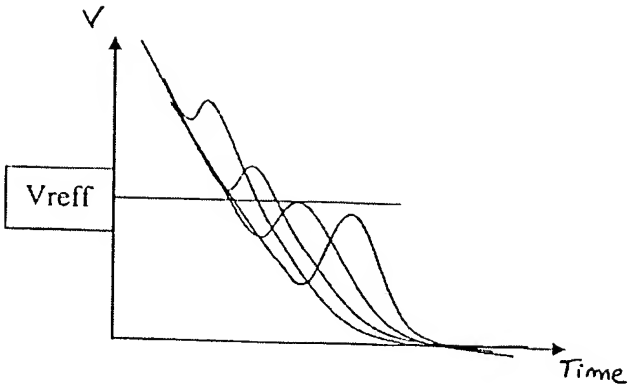


FIGURE 14A

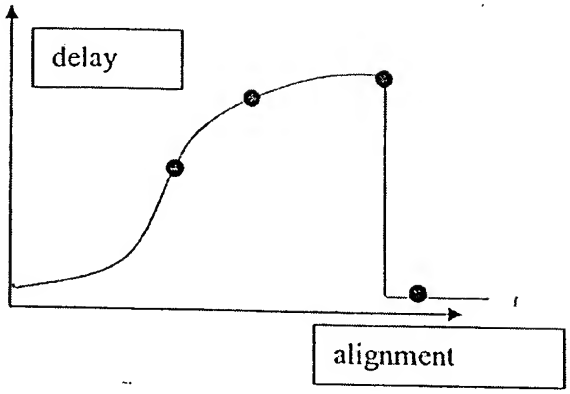


FIGURE 14B

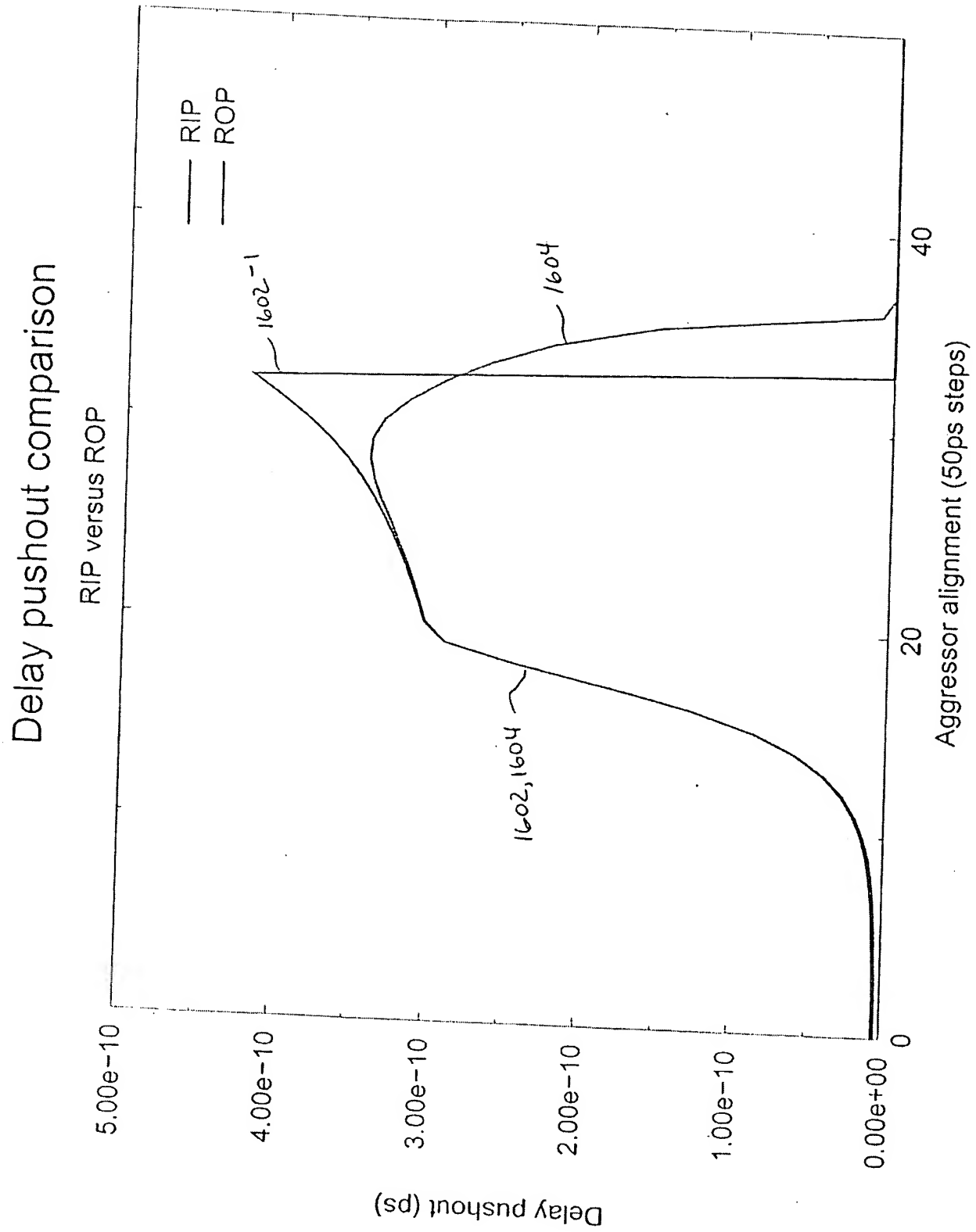

Delay pushout comparison
RIP versus ROP
RIP
ROP
1602-1
1604
1602, 1604
5.00e-10
4.00e-10
3.00e-10
2.00e-10
1.00e-10
0.00e+00
Delay pushout (ps)
0
20
40
Aggressor alignment (50ps steps)

FIGURE 15

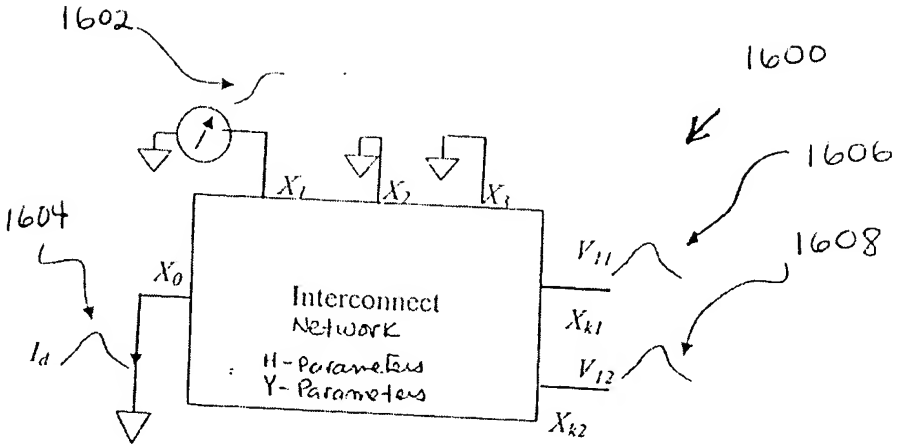

1602
1600
1606
1604
1608
X_1
X_2
X_3
X_0
I_d
Interconnect Network
H-Parameters
Y-Parameters
V_{11}
X_{k1}
V_{12}
X_{k2}

FIGURE 16